IN THE CLAIMS:

All of the pending claims 1-8 are set forth below. The status of each claim is indicated with one of (original), (previously presented), or (currently amended). Please AMEND claims 1, 3, 4, and 5 in accordance with the following:

1. (currently amended) A computer which performs parallel processing of a plurality of programs in a time-division fashion, comprising:

a memory;

an instruction fetch unit configured to fetch instructions from said memory;

hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs ~~that are not limited in number by a total hardware resource of said computer~~;

an evacuation unit which records identification information identifying a first program, and evacuates information stored in an area of said plurality of areas if the area is necessary for execution of a second program and is being used for execution of the first program, said information being evacuated ~~outside said computer~~to a portion of said memory that corresponds to the first program; and

a restoration unit which restores the evacuated information to the area based on the identification information when the second program comes to a halt or to an end.

2. (original) The computer as claimed in claim 1, further comprising an interruption unit which brings about interruption processing if the area is necessary for execution of a second program and is being used for execution of the first program, wherein said evacuation unit operates as part of the interruption processing to record the identification information and to evacuate the information stored in the area.

3. (currently amended) A computer which performs parallel processing of a plurality of programs in a time-division fashion, comprising:

a memory;

an instruction fetch unit configured to fetch instructions from said memory;

hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs ~~that are not limited in number by a total hardware resource of said computer~~;

an evacuation unit which records identification information identifying a first program, and

evacuates information stored in a first area of said plurality of areas if the first area and a second area of said plurality of areas are necessary for execution of a second program and are being used for execution of the first program, said evacuation unit subsequently evacuating information stored in the second area when use of the second area becomes actually necessary for execution of the second program, said information being evacuated to a portion of said memory that corresponds to the first program~~outside said computer~~; and

a restoration unit which restores the evacuated information to the first and second areas based on the identification information when the second program comes to a halt or to an end.

4. (currently amended) A method of controlling a computer which performs parallel processing of a plurality of programs in a time-division fashion, said computer having a memory and an instruction fetch unit configured to fetch instructions from said memory, comprising:

providing hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs~~ that are not limited in number by a total hardware resource of said computer~~;

recording identification information identifying a first program, and evacuating information stored in an area of said plurality of areas if the area is necessary for execution of a second program and is being used for execution of the first program, said information being evacuated to a portion of said memory that corresponds to the first program~~outside said computer~~; and

restoring the evacuated information to the area based on the identification information when the second program comes to a halt or to an end.

5. (currently amended) A method of controlling a computer which performs parallel processing of a plurality of programs in a time-division fashion, said computer having a memory and an instruction fetch unit configured to fetch instructions from said memory, comprising:

providing hardware resources divided into a plurality of areas, the hardware resources being used in common by a plurality of programs~~ that are not limited in number by a total hardware resource of said computer~~;

recording identification information identifying a first program, and evacuating information stored in a first area of said plurality of areas if the first area and a second area of said plurality of areas are necessary for execution of a second program and are being used for execution of the first program, followed by subsequently evacuating information stored in the second area when use of the second area becomes actually necessary for execution of the second program, said information being evacuated to a portion of said memory that corresponds to the first

programoutside said computer; and

restoring the evacuated information to the first and second areas based on the identification information when the second program comes to a halt or to an end.

6. (previously presented) A computer for parallel processing, comprising:

an evacuation unit which records identification information identifying a first program stored in one of a plurality of areas of a hardware resource being used in parallel by at least two of a plurality of programs, if the area is necessary for execution of a second program, and evacuates the information; and

a restoration unit which restores the evacuated information to the area based on the identification information when the second program comes to a halt or to an end.

7. (previously presented) A method for parallel processing comprising:

recording identification information identifying a first program stored in an area of said plurality of areas being used to run at least two of a plurality of programs in parallel;

evacuating information if the area is necessary for execution of a second program; and

restoring the evacuated information to the area based on the identification information when the second program comes to a halt or to an end.

8. (previously presented) A method, comprising:

evacuating information associated with an executing first program and identified by a first program identifier where the information is located in a first area of a processor and is evacuated to outside the processor when the area is necessary for execution of a second program; and

restoring the evacuated information to the first area using the identifier when the second program ends execution.